Q.P. Code: 16EC424 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year II Semester Supplementary Examinations February-2022

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Design CMOS transistor circuit for 2-input AND gate. With the help of function table, explain the circuit.	**7M**
	b	Design a CMOS circuit that has the functional behavior f(Z)=A.(B+C).	**5M**
		OR	
2	a	Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.	**6M**
	b	Compare Different logic families.	**6M**
		UNIT-II	
3	a	Discuss about behavioral design element with an example.	**6M**
	b	Design the logic circuit and write a data-flow style VHDL program for the following function. F (P) = ΣA,B,C,D (1,5,6,7,9,13) + d(4,15).	**6M**
		OR	
4	a	Write about structural design elements with an example.	**6M**
	b	Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c d) Also draw the relevant logic diagram.	**6M**
		UNIT-III	
5	a	Write a VHDL code for 4-bit ALU IC 74x181.	**6M**
	b	Draw the structure of a 4-bit comparator and briefly explain about it. Write a structural VHDL code for it.	**6M**
		OR	
6	a	Design a Full adder with Half adders logic circuit.	**6M**
	b	Write VHDL code for the above design in structural model.	**6M**
		UNIT-IV	
7	a	Design a 4-bit Johnson Counter and explain its operation.	**7M**
	b	What is LFSR counter and ring counter?	**5M**
		OR	
8	a	Design a bit LFSR counter using 74x194.List out the sequence assuming that the initial state 111.	**6M**
	b	Write a VHDL code for the above design.	**6M**
		UNIT-V	
9		What is a dual priority encoder? Explain. Write VHDL code for the design.	**12M**
		OR	
10	a	Distinguish between the synchronous and asynchronous counters.	**6M**
	b	Design a synchronous 4-bit up counter.	**6M**

*** END ***